

## Design of Low Voltage Low Power CMOS OP-AMP

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### ABSTRACT

Operational amplifiers are an integral part of many analog and mixed signal systems. As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. This paper presents a two stage CMOS operational amplifier, which operates at  $\pm 1.8V$  power supply using TSMC 0.18 $\mu m$  CMOS technology. The OP-AMP designed exhibit unity gain frequency of 12.6 MHz, and gain of 55.5db with 300uW power dissipation. The gain margin and phase margin of OP-AMP is  $45^\circ$  and  $60^\circ$  respectively. Design and simulation has been carried out in P Spice tool.

**Key Words:** 2 stage Op-Amp, Low voltage, Stability, frequency compensation

### I. INTRODUCTION

An Operational Amplifier is a high gain differential amplifier which can be used as summer, integrator, differentiator etc. Operational Amplifiers are an integral part of many analog and mixed signal systems. In designing an Op-Amp, numerous electrical characteristic e.g, gain bandwidth, slew rate, common mode range, output swing offset all have to be taken in to account. Since the op-amps are designed to be operated with negative feedback connection, frequency compensation is necessary for closed loop stability. Research indicates that major performance measures such as DC gain, GBW, and PM of an amplifier are greatly influenced by the design of the input stage [1-10]. Because of this, there has been much focus on the optimal design of the input stage to keep these performance measures constant across the common-mode range. Most of the focus has shifted towards the argument of keeping gm constant, but the overall intent is to obtain a constant operation for all amplifier specifications. Many designs use the same architecture, but make changes to the input stage to obtain a rail-to-rail input stage and constant operation. A commonly used architecture for low voltage amplifier designs is a two stage amplifier. This architecture is used because it maximizes the ability to manipulate the input stage to achieve the rail-to-rail operation that is desired in low voltage design. A commonly used technique for the input stage is the implementation of a complementary input pair. This means that the input consists of an n-ch input pair as well as a p-ch input pair. Implementing this technique insures that at least one input pair is operating when the common-mode shifts near the supply rails. However, the use of complementary input pairs does not insure that there will be a constant operation across the common-mode range. For stability Miller compensation is used.

Power dissipation can be reduced by reducing either

supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. Another concern that draws from supply voltage scaling is the threshold voltage of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues. In order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology.[1].This paper presents different topology for designing a low power two stage cmos op-amp.

### II. Block Diagram of Two Stage CMOS Op Amp

Two-stage OP-AMP mainly consists of a cascade of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. Figure 1 shows the specific two-stage CMOS op-amp. The second stage is also nothing more than the current sink inverter.[10] The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption. If the Op -Amp must drive a

low resistance load the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing. Bias circuit is provided to establish the

operating point for each transistor in its quiescent stage. Compensation is required to achieve stable closed loop performance.

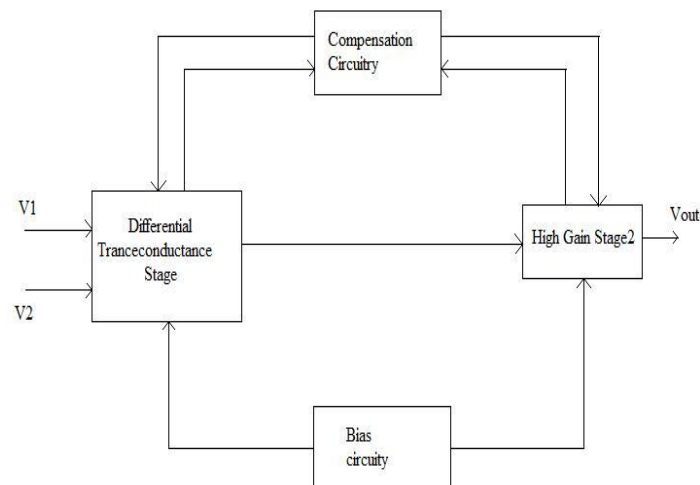


Figure (1): Block Diagram of Op-amp

### III. Two Stage CMOS Op Amp Circuit

Operational Amplifiers plays essential role for many analog circuit designs. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp. If the gain and bandwidth is large, the speed and accuracy of amplifier will be high. The topology of this circuit is that of a standard CMOS op-amp. It comprised of three subparts, namely differential gain stage, second gain stage and biasing network. It was found that this topology was able to successfully meet all of the design specifications.

The circuit diagram of two stage CMOS Op amp is shown in figure 2. It consists of total 9 transistors with a load capacitor and a compensation capacitor. Transistors M1, M2, M3, and M4 constitute the first stage of op amp which is the differential amplifier. The gate of M1 is the non inverting input and the gate of M2 is the inverting input. A differential input signal is applied across the two input terminals will be amplified according to gain of differential stage. The gain of this stage is the transconductance of M1 times the total output resistance seen at the drain of M2. The main resistance that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the load transistors, M3 and M4. The current mirror active load used in this circuit has three main advantages.

First the use of active load devices create a large output resistance in a relatively small amount of chip area. The current mirror topology performs the differential to single- ended conversion of the input signal, and finally the load helps with common mode rejection ratio. In this the conversion from differential to single- ended is achieved by using a current mirror M4 and M3. The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. Finally the differential current from M1 and M2 is multiplied by the output resistance, which is the part of the input to the next stage.

The second stage is a current sink load inverter. The aim of the second stage is to provide additional gain consisting of transistor M6 and M7. This stage receives the output from the drain of M2 and amplifies it through M6 by common source configuration. This stage employs an active device, M7, which serve as the load resistance for M6. The gain of this stage is the transconductance of M6 times the equivalent load resistance seen at output of M6 and M7. M6 is the driver while M7 acts as load. Transistor M8 and a reference current source form a simple current mirror biasing network that provides a voltage between the gate and source of M5 and M7 sink a current based on their gate to source voltage which is controlled by the bias network.

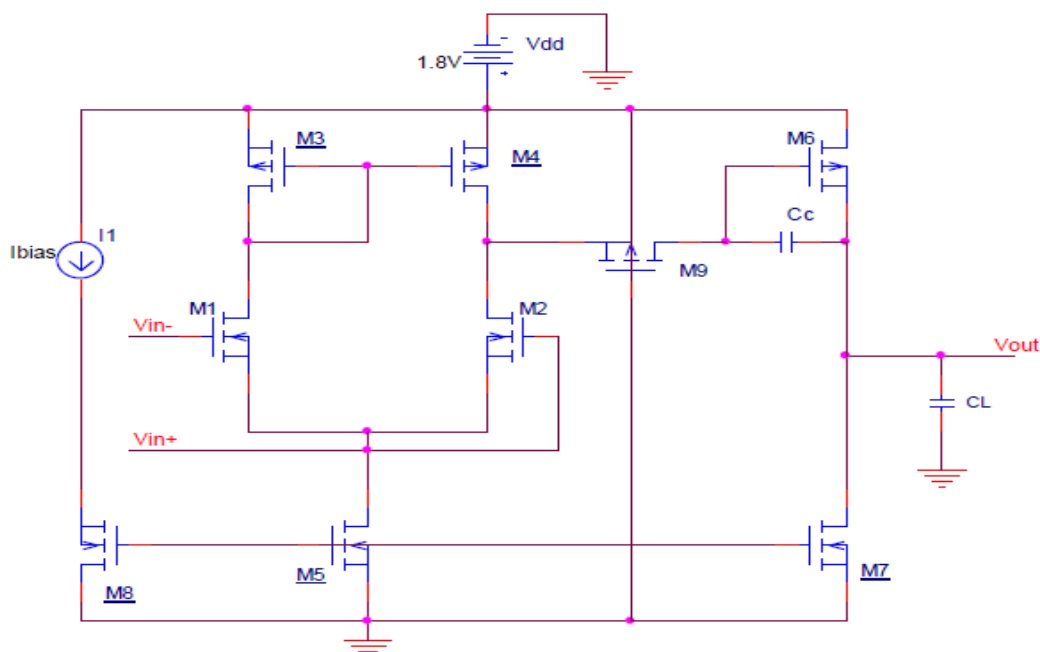


Figure (2): Circuit diagram of Two stage Op amp

#### IV. Design Specification

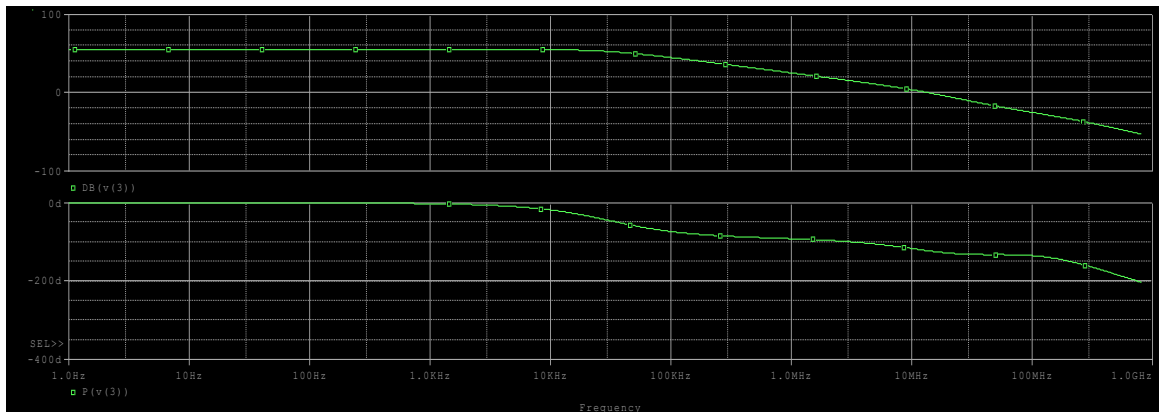
The first aspect considered in the design was to meet the desired specifications. Based on a clear understanding of the specifications, we have chosen the standard CMOS op-amp circuit topology in our design. The design specification of operational amplifier is shown in table 1. The compensation capacitor is designed to achieve stability. This compensation capacitor is connected in series with a resistor which is implemented with a PMOS. In a two stage op-amp circuit design, in order to get stability in the system, proper compensation techniques should be added with the op-amp circuits. There are several compensation techniques available like pole splitting miller compensation, self compensating capacitor, feed forward compensation using an additional amplifier, negative miller compensation. In comparison with various compensation techniques RC miller compensated technique provides high gain and voltage swing and has been used in this two stage op-amp circuit.

TABLE1.  
 Specification of two stage CMOS Op amp

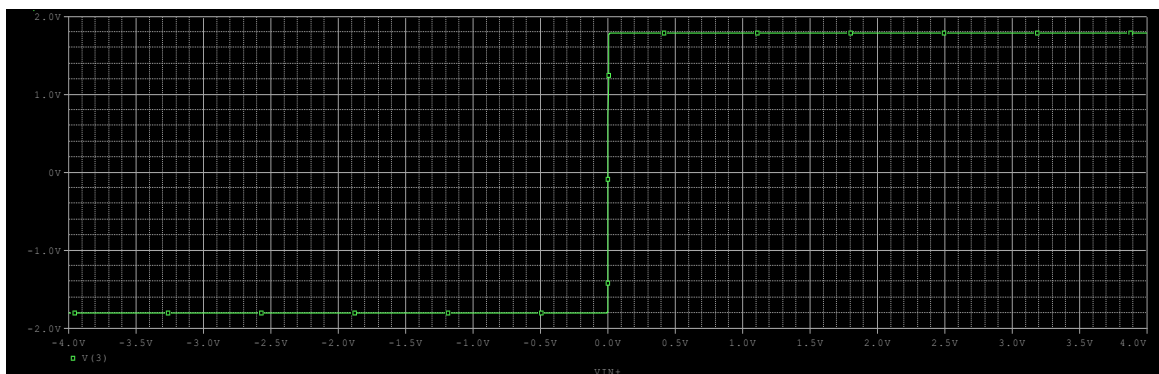
Specification Names	Values
Supply VDD	$\pm 1.8V$
Gain	$\geq 60dB$
Gain Bandwidth	5MHz
Power dissipation	$<100\mu w$
Slew Rate	10V/usec
Input common Mode Range	0.6V – 1.8V
Phase Margin	$65^\circ$
Output Swing	-1.8V – 1.8V
$C_L$	10pf

## V. Simulation and Result

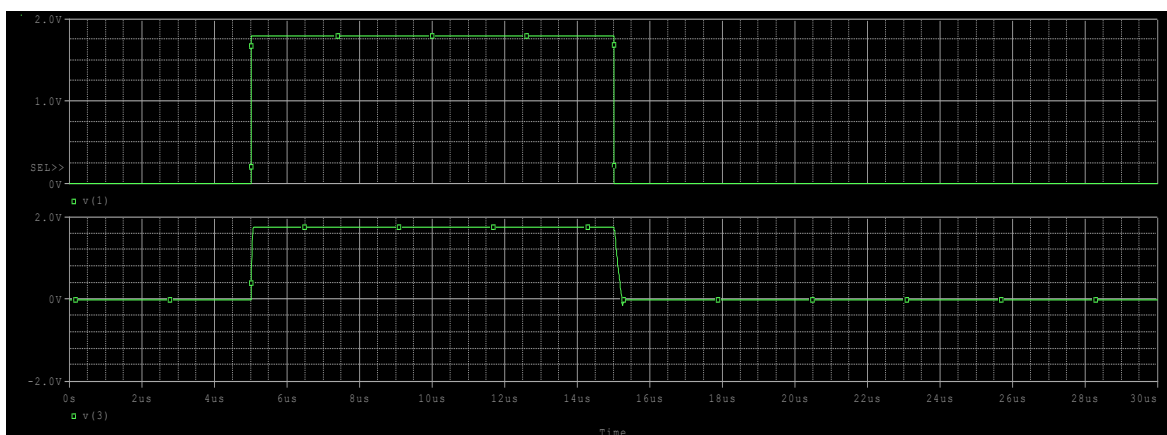
### 5.1 AC Response



### 5.2 Output Swing



### 5.3 Transient Response



**TABLE 2**  
**Simulated result**

Specification Names	Result
Supply VDD	$\pm 1.8V$
Gain	55.5dB
Gain Bandwidth	12.6MHz
Power dissipation	300uw
Slew Rate	0.3V/usec
Input common mode range	-1.8V – 1.8V
Phase Margin	60°
Output Swing	-1.8V – 1.8V
Output resistance	28k $\Omega$

### VI. Conclusion

The two stage CMOS Op amp has been designed and its behavior is analyzed. Simulation results confirm that the proposed design procedure can be utilized to design op amp. The simulation is done with Pspice Software. The design is on 0.18 $\mu$ m technology. The Op amp is designed with low power of 300uw and gain of 55.5db and gain bandwidth of 12.6 MHz and Slew rate is 0.3V/us.

### VII. Future Scope

Design of accurate A/D converters and filters are challenging work for present applications. So this work can be extended further for communication applications with improved slew rate .For the mixed integrated circuit unity gain bandwidth can be further increased.

### REFERENCES

[1] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design" Oxford University Press, 2nd edition.  
 [2] D. A. Johns and K. Martin, "Analog Integrated Circuit Design," New York: John Wiley & Sons, Inc., 1997.  
 [3] Amana Yadav, "A Review Paper On Design And Synthesis Of Two stage CMOS Op-amp" ©Ijaet Issn: 2231-1963677 Vol. 2, Issue 1, Pp. 677-688  
 [4] B. Razavi, "Design of Analog CMOS Integrated Circuits," Tata McGraw-Hill, 2002.  
 [5] Ankit Sharma, Parminder Singh Jassal, "Design Of A Ultra Low Power, High Precision CMOS Opamp Based Comparator For Biomedical Applications", International Journal of Engineering Research and

Applications (IJERA) , Vol. 2, Issue 3, May-Jun 2012, pp.2487-2492

[6] R Lotfi, M Tahenadeh-Sani, M Yaser Asizi, and O. Shaaei. "A 1-VMOSFET-only Fully Differential Dynamic Comparator Used in Low Voltage Pipe Lined AID Converter,"  
 [7] Ehsan Kargaran, Hojat Khosrowjerdi, Karim Ghaffarzadegan "A 1.5 V High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18  $\mu$ mTechnology ," 2010 2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010).  
 [8] Purvi .D Patel, Kehul . A Shah "Design of low power two stage CMOS Operational Amplifier".(IJSR)ISSN23197064.  
 [9] P.K.Sinha, Abhishek Vikram, Dr. K.S.YADAV, "Design Of Two Stage CMOS Op-amp With Low Power And High Slew Rate." (IJERT) Vol. 1 Issue 8, October - 2012  
 [10] Priyanka Kakoty, "Design of a high frequency low voltage CMOS operational amplifier", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011